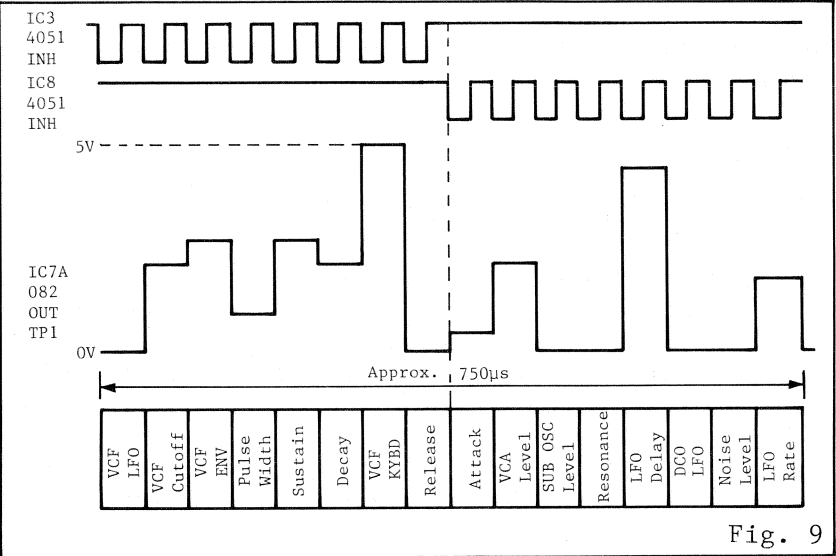


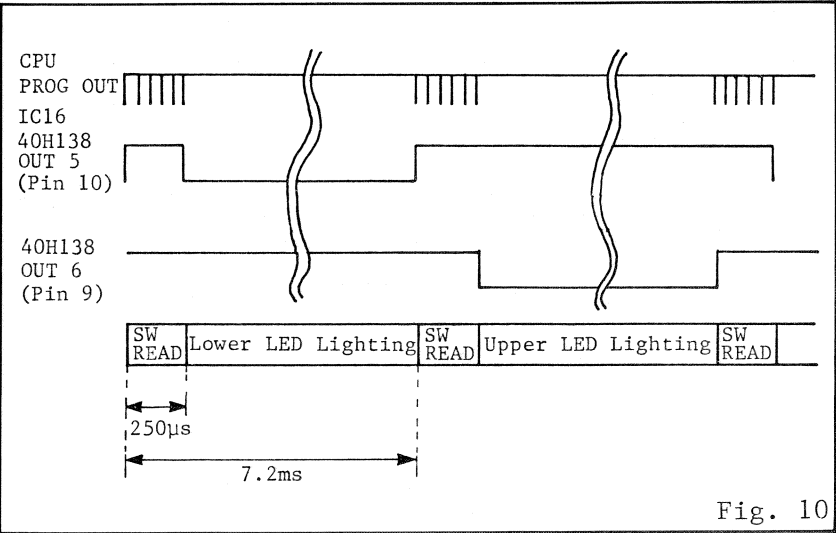
POT DATA OUTPUT

An 8-bit data representing pot setting is placed on the CPU bus 16 times for each pot. Each 8-bit is latched by IC13, D/A converted by R-2R and sent to IC3 and IC8 (POT DMPLXER) on Board A, where it is distributed to a channel addressed by port 2.0-2.3 of the CPU (Board B) at a sampling rate of INH from IC19 (Board B).



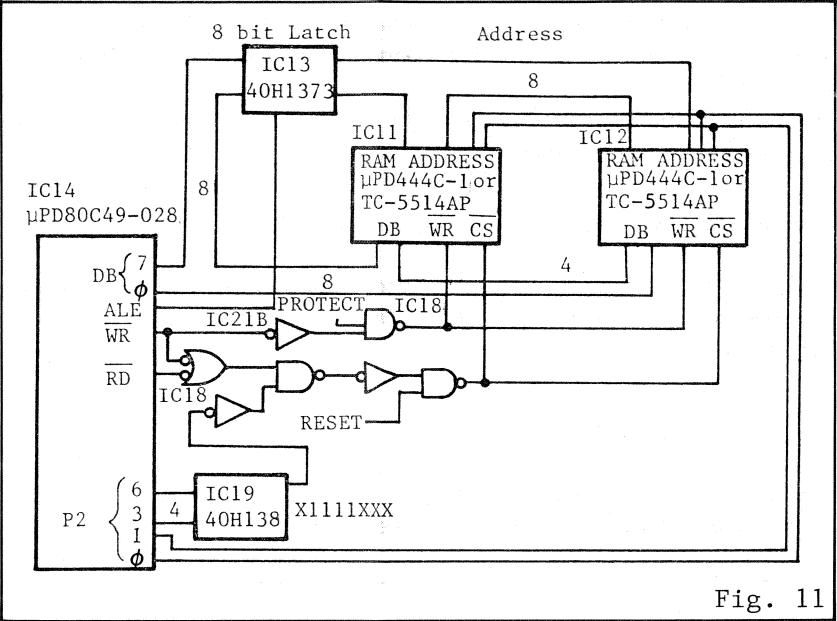
DISPLAY LED LIGHTING

Being an I/O port, the Port 1 changes its state to output mode immediately after finishing switch readings, delivering display LED driving signals to LED board. Alternately swinging outputs (pins 9 and 10) of IC16 allow upper and lower LEDs to conduct at duty cycle of nearly 50 of dynamic lighting. The period 7.2ms in the timing chart (Fig. 10) is the time required for the CPU to complete one program loop.



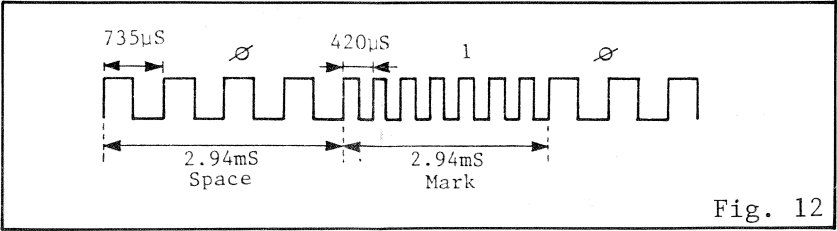
MEMORY

Two identical RAMs (4K bit — 4x1024) make up the patch memory, which can store up to 1K byte (8x1024 words). Each memory cell is addressable with 10 bits. MSB 2 bits come from ports 2.0 and 2.1. The remaining LSB 8 bits from Data bus are latched into RAMs by IC13 with ALE. RAM chip select (CS) is accomplished under the conditions
Port 2 = X1111XXX
WR or RD = low
RESET = high.
The CPU can extract RAM memory only when WR is ANDed with PROTECT at IC18.



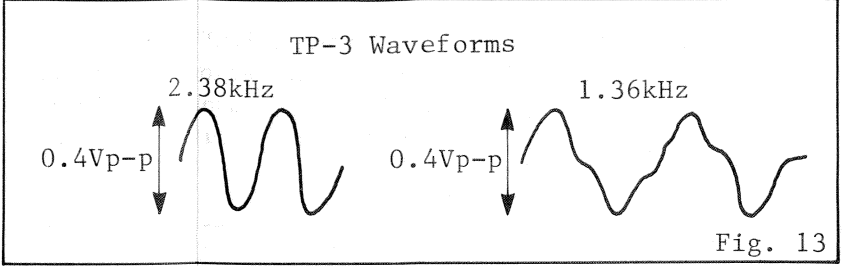
TAPE INTERFACE

The CPU (Board B) transfers the programmed data to or from a cassette recorder through Interface circuitry at approx. 340 baud (340 bits/s).



SAVE

Pressing SAVE button allows the CPU to convert a set of patch data bits to square waves: 0 (space) to four cycles of 1.36kHz and 1 (mark) to seven cycles of 2.38kHz, and to send them from Port 2.7. The modulated bits are applied through IC21E (inverter) to IC22A (LPF) where their high order harmonics are rolled off by 12dB/oct slope and lower components by C22 (6dB/oct HPF) before being passed on to SAVE jack.



LOAD & VERIFY

Data from tape reach TO of the CPU by way of C23 x R82, HPF to eliminate DC component and fluctuation; IC23A, amp and LPF (12dB/oct); IC23B, comparator to have their shape restored to rectangular whose wavelength enables the CPU to perform calculation on the input wave lengths to determine the bits value (0 or 1). The tape interfacing directly involves the software and forces the CPU to stop most of other jobs (lighting display, refreshing S/H, reading pots and switches). During the tape modes output 0 (pin 15) of IC16 (decoder) is clamped to low to let a tape mode indicator light up and to allow the CPU to escape from the tape routine when MANUAL is pressed.

DCB (Digital Communication Bus)

The JUNO-60 can be controlled from the external equipment which transmits the control voltage in the form specified in this section. The JUNO-60 can also control an external "musical instrument" which accepts data made in the form described in this section. The CPU on the CPU Board communicates with an external equipment through DCB (Digital Communication Bus). IC24 on the Panel Board B interfaces them (CPU and EXT instrument).

INTERFACE

The IC24 is the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. In the JUNO-60 the 8251A is configured as Asynchronous Receiver/Transmitter (USART). The 8251A will signal the CPU (on the CPU Board) whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of 8251A, when INT goes low under one of the following conditions, by turning C/D to high (1) and READ to low (0), entering Interrupt Handling Routine.

INT LOW CONDITIONS: RxRDY — 1 (H)
or TxEMPTY — 1 (H) and TX BUSY — 1 (H)
(DCB connector)

* RxRDY: 1 (H)
This output indicates that 8251A contains a character that is ready to be input to the CPU, requiring the CPU to accept the data.

* TxEMPTY: 1 (H) & TX BUSY: 1 (H)

When the 8251A has no characters to transmit, TxEMPTY will go "high" which is inverted by IC27D (Panel Board B) and applied to pin 4 of IC27C. If the receiving party is transmitting RX BUSY (which is a low TX BUSY at the JUNO-60's DCB connector), IC27C cannot turn IC27B output to low, having INT signal remain low.

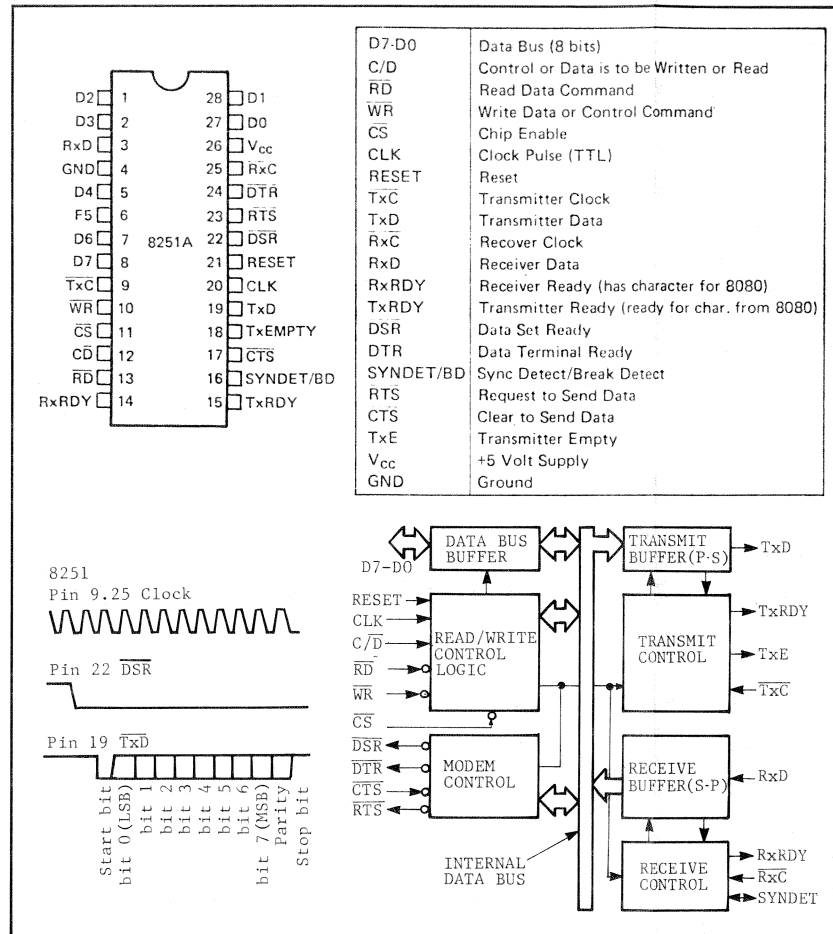


Fig. 14

DCB DATA FORMAT

The Data format described in this section is commonly applicable to Roland products furnished with the DCB connector. Variations unique to individual models and problems which might happen in linking the JUNO-60 to other DCB instruments will be discussed in more detail later.

GENERAL SPECIFICATIONS

* BLOCK

Basically, a block is comprised of three codes: one Identifier, one or more Data Codes and one End Mark. The transmitter can send a block (containing identical information) either continuously or intermittently at 10ms–100ms intervals to assure stable information transmission. In an interval transmission system, the transmitter must send a new block upon occurring of change in the information. The new block must contain both changed and unchanged data.

* IDENTIFIER

At the head of each block is a 1-byte identifier which uses a value within 0F1H (241) through 0FEH (254) to signify the kind of DATA CODE that follows. 0FDH (253) – PATCH CODE, 0FEH (254) – KEY CODE, others are undefined. Any data which follows an Identifier must not include these values.

* DATA CODE

A Data code is comprised of one section or series of sections (each 1 byte, called channel—CH) containing the information defined by the identifier. The code length (number of channels) depends on circuit configuration of the transmitter. Once a communication is established over DCB, the code length and the transmission order of the channels should not be changed throughout the communication.

Some identifiers will be accompanied by the code of predetermined length. (Exp. PATCH CODE—1 byte.)

* END MARK

An End Mark is necessary unless the code length is predetermined by the identifier or the block is to be automatically terminated by the identifier of the next block.

* DATA PROCESS

The receiver begins processing data code at the moment it accepts the End Mark or the Identifier at the head of the next block.

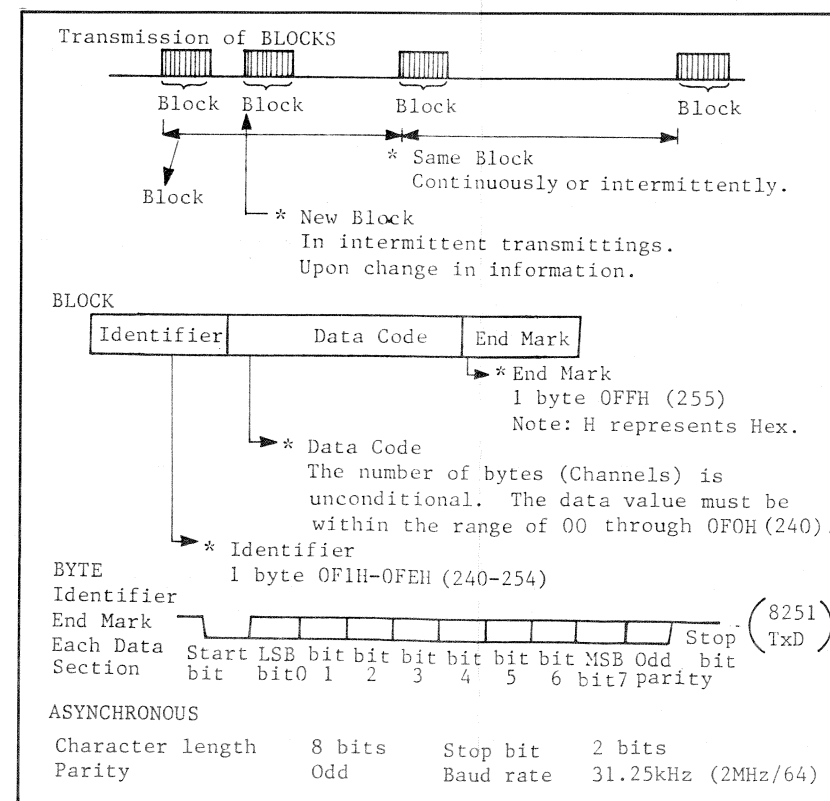


Fig. 15

DETAILED SPECIFICATIONS

This part mainly discusses the Key Code, only which the JUNO-60 deals with and problems that may arise in linking the JUNO-60 with other DCB instruments, e.g. OP-8 and JP-8. Some differences in the data format and transmission will exist between models.

* BLOCK

The JUNO-60 transmits blocks continuously, while the JP-8 and OP-8 intermittently.

* IDENTIFIER

Two Identifiers are already defined:

0FDH (253): Patch Code

Indicates that the code is 1-byte format representing Patch Number or Patch Preset Number.

This code is employed in the JP-8 and the OP-8. The JUNO-60 does not deal with this code. It ignores the data following this identifier.

0FEH (254): Key Code

This signals the receiver that the following data is for key information (key number and gate).

The length of the data:
JP-8 and OP-8 — 8 bytes
JUNO-60 — 6 bytes

* DATA CODE

Patch Code

The JP-8 and OP-8 send this code together with the Key code for each change in Patch data and do not transmit it again. This block does not accompany End Mark.

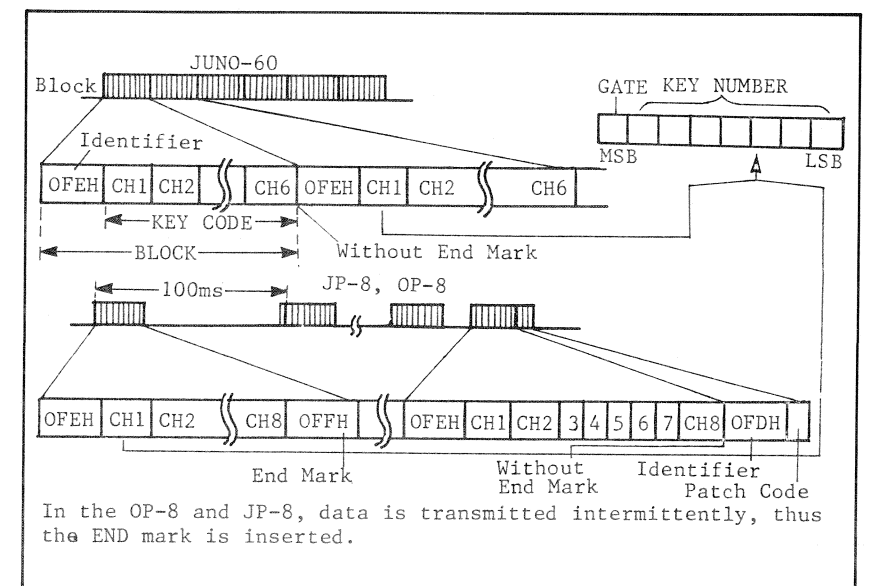


Fig. 16

Key Code

The Key Code is preceded by the Key Code Identifier (0FEH 254). Since the JUNO-60 is so configured that it accomodates only Key Code, the CPU (CPU BRD) returns to the main routine if identifier bits is other than 0FEH, ignoring the subsequent data.

The transmitter assigns the keys played on its keyboard to individual channels, coding each key information in 8-bit format where MSB 1 bit represents GATE ON (1) or OFF (0). The remainder (7 bits) represents key designation (name) listed in the table below (Fig. 17) (Hexa-decimal). Then, the transmitter places all the channels on the DCB sequentially in the order of its key assign mode. The receiver, upon receiving channels, assigns its voices to them by its own key assign mode which will differ between models. Fig. 17 shows some rather distinguishable key assignments. The transmitter need not delete the unnecessary channel(s), instead it turns MSB to 0 (GATE OFF).

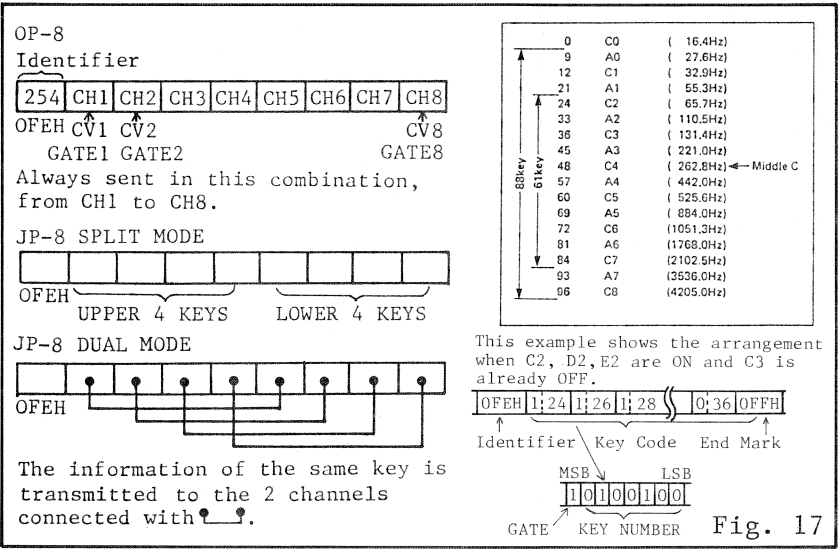


Fig. 17

KEY ASSIGN TO BUILT-IN & EXTERNAL KEYBOARDS

When "external keyboard" is connected to the JUNO-60 through the DCB, the CPU recognizes it as one being connected to the built-in keyboard in parallel and assigns its voices to whichever the key played on both keyboards. However, if two keys of the same note are played at a time on both keyboards, the program gives priority to the key first played as long as the GATE is ON. This fact may trick the player when he plays the JUNO-60 with SUSTAIN set shorter than the gate duration of the note being reproduced. For example, if he plays C4 right after the C4 note activated by DCB dies away, it doesn't sound. To retrigger the gate both keys must once be made OFF, then one key is pressed again.

KEY CODE INCLUDING MORE THAN SIX CHANNELS

What will happen if more than 6 channels are fed from the external keyboard to the JUNO-60? In this case, of course, 7th and subsequent keys have to wait until reserved channels are cleared, either by releasing of keys or by software. The software steals a voice from a channel whose gate first turned ON among 6 channels. Then the program assigns the voice again to 7th channel and so on as long as new channels are coming. This featue enables the JUNO-60 to accept limitless channels within a key code. Contrast to this, the JP-8 can receive 8 channels only at a time.

LINKING DCB DEVICES

Two cables are available for connecting DCB units, DCB Cable H172 and H165.

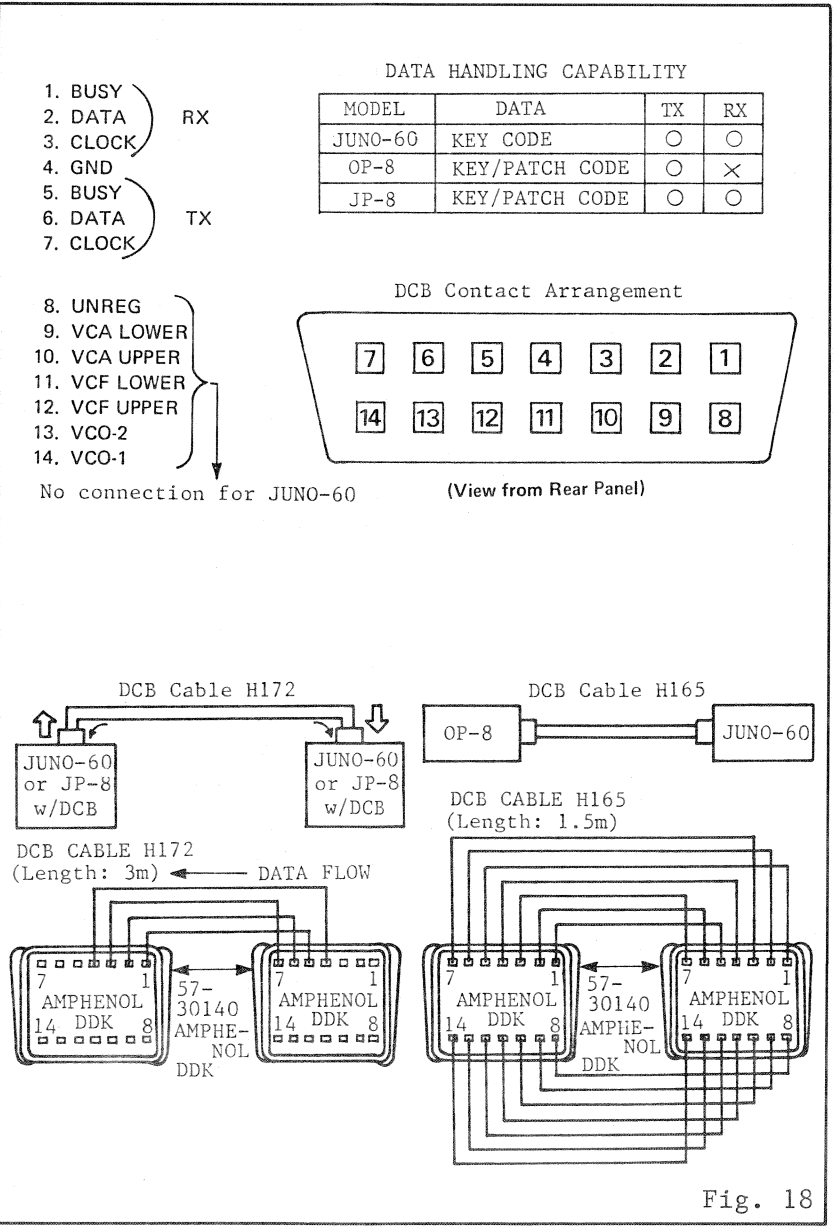
DCB Cable H172 is uni-directional, with the signal-flow direction shown by the arrow on the connector.

When connecting two JUNO-60 or JP-8 units, be sure to connect the cable so that the arrow points away from the JUNO-60 or JP-8 unit to be played, and towards the JUNO-60 or JP-8 unit to be controlled.

Also, when controlling the JUNO-60 with the OP-8, DCB Cable H172 can be used to connect the OP-8 to the JUNO-60.

Be sure to connect the cable so that the arrow points away from the OP-8 and towards the JUNO-60. Otherwise, the JUNO-60 may operate incorrectly.

On the other hand, DCB Cable H165 is a bi-directional cable in which sent from the TX-terminal on a unit returns to the RX-terminal on the unit, causing regeneration.



GROUND LOOP NOISE

Because of the AC ground, a "ground loop" may be created when the DCB cable is connected between the JUNO-60 and its party (equipment). As a result, a certain-level digital noise may occur. In the later JUNO-60 the noise is considerably reduced by rearrangement of ground paths together with installation of Panel Board B of improved version, 052H411C (pattern relayout).

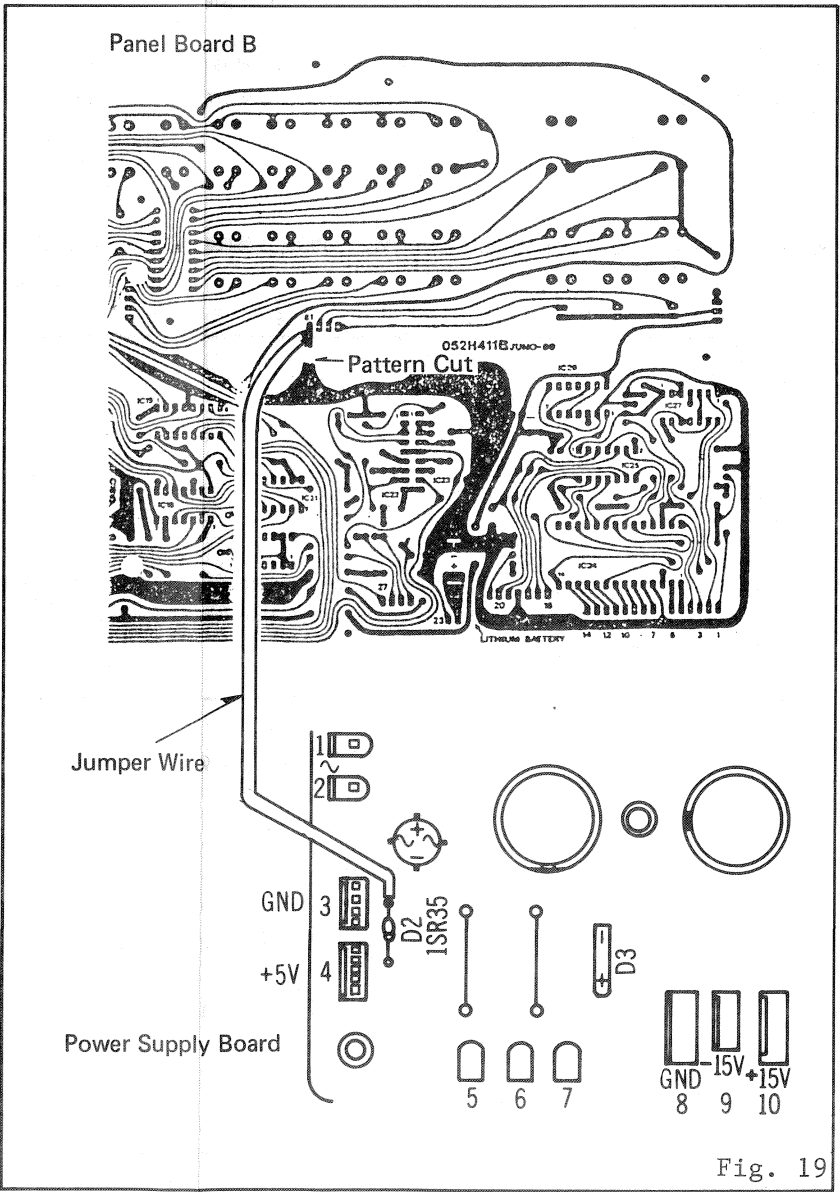
The modification is conducted at the factory on the units with serial numbers 253800 and subsequent.

For the units prior to SN253800, alternative modification can be made for the purpose of noise reduction.

See Fig. 19.

Note: This modification has no effects on the later units.

Caution: Do not disconnect GND from DCB connector (Pin 4). Floating digital GND path may induce noise in other signal path.



RAM MEMORY TEST

The JUNO-60 has RAM TEST Program. In the RAM test mode, the program writes to each RAM chip and reads the data back to find any defective memory cell that may exist in the RAMs. If there is an error, the memory address will be displayed in the PATCH NUMBER window in Hexadecimal figure, as exampled below. (Fig. 21)

Caution: * All programmable data will be erased during the test. Save them on tape before testing.
* RAM should not always be defective if indicated by "error display". Check DATA BUS and their associated ICs, Trs, etc. for short or open.

HOW TO RUN TEST PROGRAM

1. Set controls as indicated by arrow.
2. Insert a bare plug into PATCH SHIFT jack on the rear panel to open the circuit.
3. While pressing CHORUS OFF and II buttons, switch the power on.

The program starts with the lowest address, so if a RAM is seriously defective, it displays "00" and stops there. When program sees an error, it won't step to the next address unless correction is made.

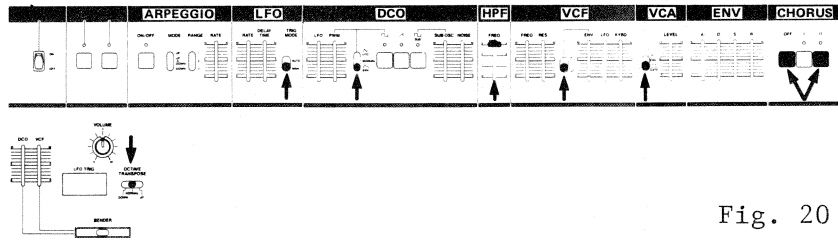


Fig. 20

If no defect is found in the RAM during the test, write data 81 (a continuous square wave sound) into all of the tone numbers so that Manual symbol  will be displayed in the LED Display.

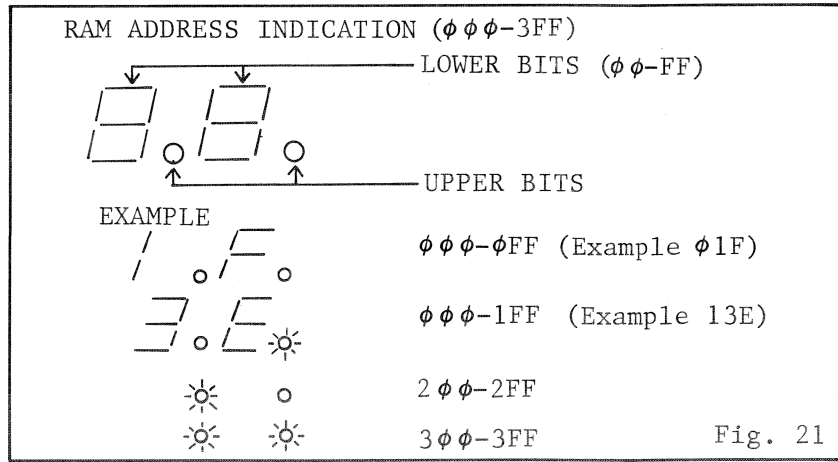
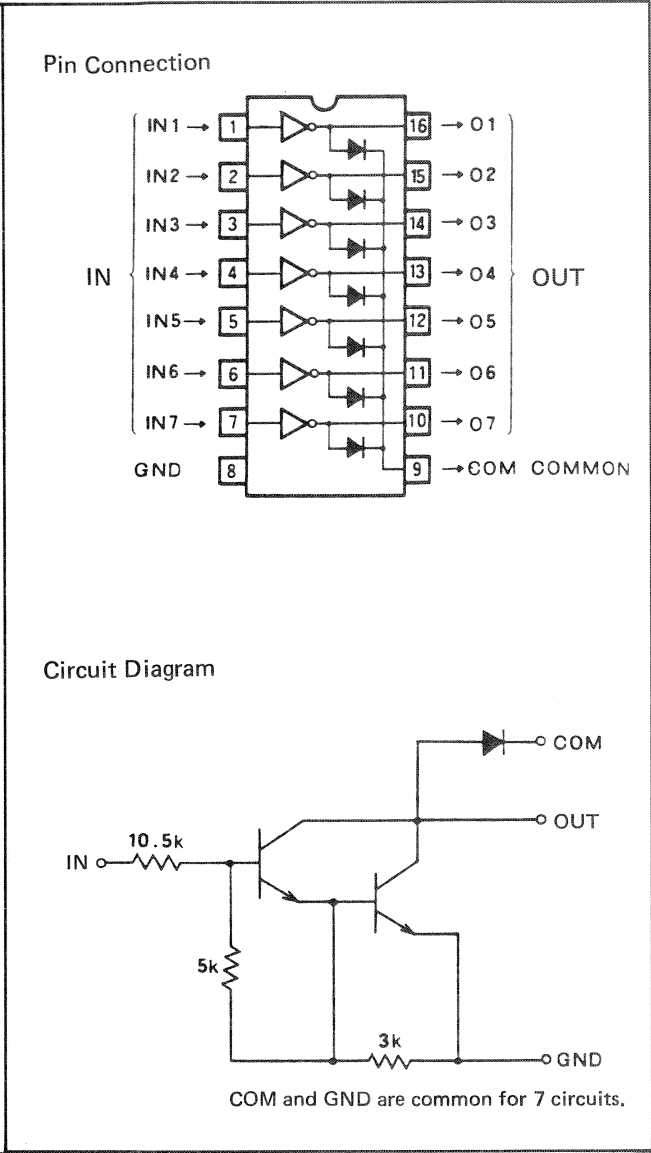
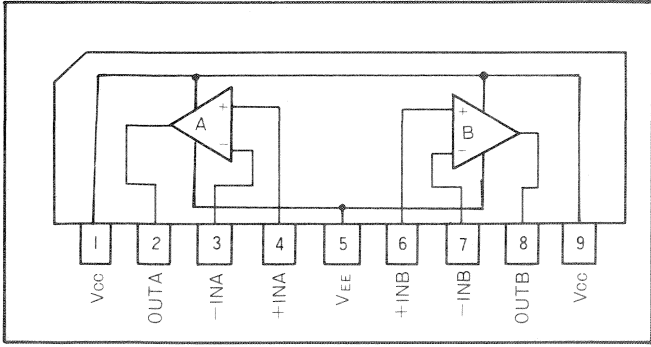


Fig. 21

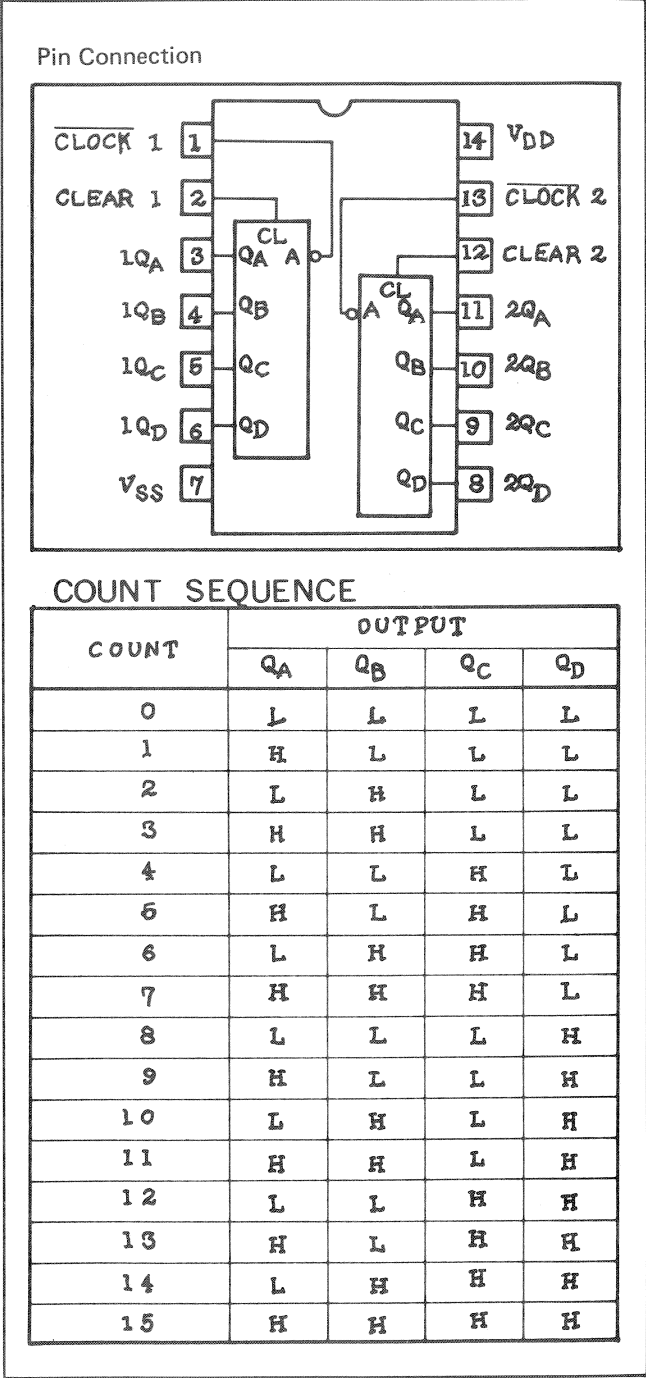
M54528P
7-Segment Driver



TA75558S
TA75559S
OP-Amp



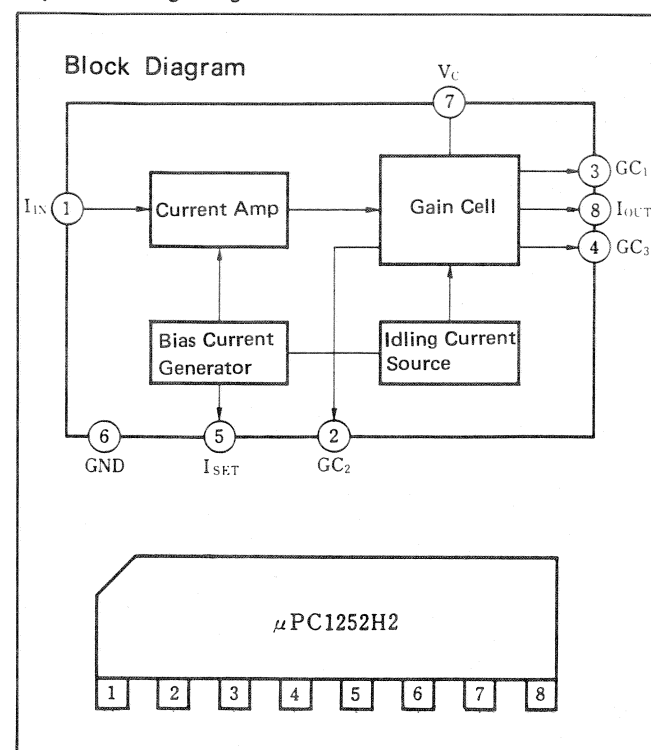
TC40H393P
Dual 4-bit Binary Counter



COUNT SEQUENCE

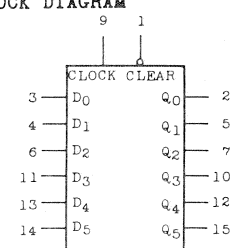
COUNT	OUTPUT			
	QA	QB	QC	QD
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

μPC1252H2
Bipolar Analog Integrated Circuit



TC40174BP

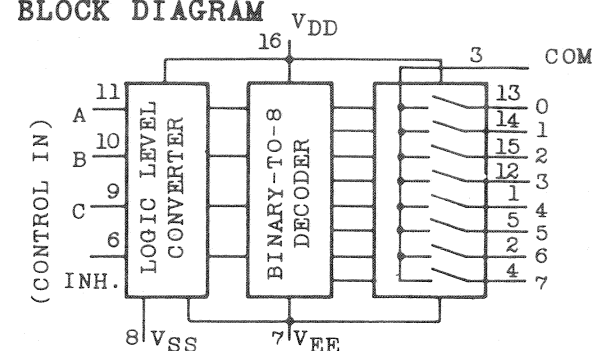
Hex D-Type Flip-Flop

 $V_{DD} : 16, \quad V_{SS} : 8$

INPUTS			OUTPUT
CLOCK Δ	D_n	CLEAR	Q_n
	H	H	H
	L	H	L
	X	H	Q_n^*
X	X	L	L

- △ : Level change
- : No change
- ※ : Don't care

BLOCK DIAGRAM



CONTROL INPUTS				"ON" CHANNEL
INHIBIT	C	B	A	TC4051BP
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	※	※	※	NONE
※ Don't Care				Except TC4052BP

The diagram shows the pin configuration for the 74VHC04 hex inverter. The top half of the package has pins 14 (VDD), 13 (Y0), 12 (Y1), 11 (Y2), 10 (Y3), 9 (Y4), 8 (Y5), and 7 (Y6). The bottom half has pins 1 (A), 2 (B), 3 (C), 4 (G2A), 5 (G2B), 6 (G1), 7 (Y7), and 8 (VSS). The truth table below defines the logic for each output Y based on the inputs A, B, C, G2A, and G2B.

INPUTS					OUTPUTS								
ENABLE			SELECT										
G1	G2A	G2B	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	*	*	*	*	*	H	H	H	H	H	H	H	H
*	H	*	*	*	*	H	H	H	H	H	H	H	H
*	*	H	*	*	*	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	H	L	L	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	L	H	H	H	H	L	H	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H	H
H	L	L	L	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

* : Don't care

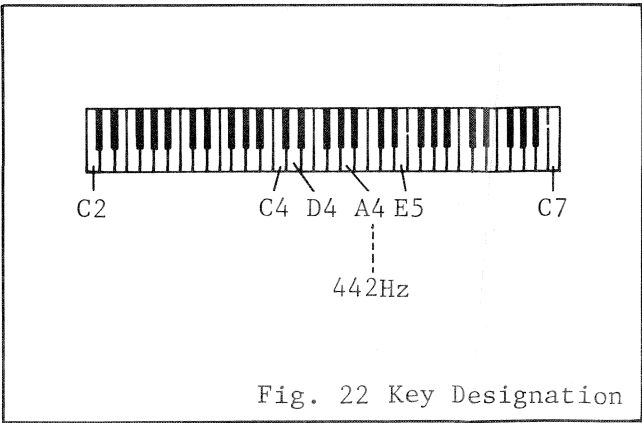
ADJUSTMENT SUMMARY

IMPORTANT:

- * Use an oscilloscope unless otherwise specified.
 - * Before starting the adjustment procedures, check the power supply voltages.
 - * These adjustment procedures assume that the JUNO-60 has not yet been adjusted at all. When adjusting a particular section, be sure to confirm that the adjustments for previous sections which may affect the present section adjustment results have been completed. For example, for the VCF adjustments, if the waveform is to be checked at either the VCA OUTPUT or the OUTPUT jack, then the VCA adjustments must have been completed.
- Table 5 below shows interrelated adjustments and those adjustments which must be performed when IC(s) or related parts of the circuit are modified.

Circuit (Stage)		Adjustment Items	
CPU BOARD			
MASTER OSCILLATOR	2-1	BIAS	
	2-2	TUNE	
	3	BENDER	
WAVEFORM	4	SAWTOOTH	
	9	PWM	
PANEL BOARD A			
LFO (IC11/IC14)	7	LFO	
	8-6/8-7	VCF LFO	
KCV (IC24)	8-3/8-4	KYBD	
ENV (IC23)	8-8/8-9	VCF ENV	
VCF CV MIX (IC20)	8-2	FREQ	
DCO LFO (IC13)	7-2	GAIN	
	7-3	OFFSET	
VCF LFO (IC21)	8-6/8-7	VCF LFO	
VCF	8-1/8-2/8-5	VCF	
	(Affected channel only.)		

Table 5



TEST PROGRAM

For easier adjustment, the two CPUs in the JUNO-60 store the Test Programs. The JUNO-60 ADJUSTMENT PROCEDURES basically use these Test Programs. However, if no Test Mode (or Patch Number) is specified for a particular adjustment, the adjustment is to be performed manually.

TEST MODES

1. Key Assign (CPU BOARD)

To enter the Test Mode, hold the KEY TRANSPOSE button down, turn the Power ON, then continue holding the KEY TRANSPOSE button down for 2 seconds. The 3 Key Assign Modes can be selected through the ARPEGGIO MODE selector.

UP (UNISON): Six voices are assigned to the same key simultaneously.

UP & DOWN (ROTARY): The CPU assigns channels (voices) in a cyclic order (i.e., 1, 2, ... 6, 1, etc.) to the keys (or repeatedly-struck single key) being played (legato or staccato) and remembers the last channel even after the key(s) is released. New assignment will start with the next channel. Note that the first key does not always activate CH1.

DOWN (NON-ROTARY): If a second key is pressed while one key is pressed, CH2 is activated. If any preceding keys are open, the channel with the smallest number takes priority for the next assignment. For example, if any 4 keys are pressed, (activating CH1-CH4), then 3 keys released (including the first key), and one key again pressed, CH1 will again be activated.

To escape the Test Mode, turn the Power OFF and wait 3 seconds before turning the POWER ON again.

Note: There are 2 adjustment methods; (1) using test point TP4, etc., and (2) listening to a sound(s) through the OUTPUT jack. Also, CH2-CH4 can be adjusted by listening to the beat sound between channels. Perform these audible adjustments in the NON-ROTARY Key Assign Mode by setting ARPEGGIO to DOWN. For example, in order to produce sounds at CH1-CH4, sequentially hold keys 1 through 4, and release keys 2 and 3. (Fig. 23) If HOLD button remains ON, an extraneous sound will be heard. Turn HOLD button OFF as necessary.

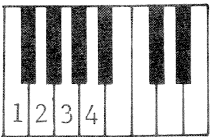


Fig. 23

2. Patch Number (PANEL BOARD B)

Insert a bare plug into the PATCH SHIFT jack in order to open the Jack Circuit. The CPU on the Panel Board B then enters the Test Mode, displaying a meaningless "11" in the Patch Number Display window. As a result, the Panel Setting Programs used for the adjustments, which are stored in BANKs 8 and 9, can be read. To call BANK 8, hold BANK button 5 down and press 3.

Note: The Patch Number does not have to be set unless otherwise specified.

Edit Mode

In the Test Mode, once a Patch Number is selected, the visual panel setting has no relation to the sound being re-

produced. However, some panel controls may need resetting for editing purposes, since the same Patch Number may be used as the basic setting for several adjustments. For example, when a control is to be set to "1" and the control is already in position "1", it may actually be set to "3" by the CPU. In this case, move the control until the 2 dots in the Patch Number Display window light up, then return the control to "1".

Caution: Before performing adjustment, check to see if the Edit Mark is displayed in the Patch Number Display window. If the Edit Mark is displayed, select any other number, then again select the desired Patch Number.

N U M B E R	NAME	T R A N S P	LFO			DCO								H I F	VCF					VCA		ENV				C H O R U S	
			R A T I O	D E L T A	M O D E	L F O	P W M	M O D E	P U L S E	S A W T H	S U B T O	S L O W B E L	N		F R E Q	R E S O	P O L A	E N V	L F O	K E Y / B D	E L E V L	A	D	S	R		
81	B-1	N	6.5	0	A	0	0	M	O N			0	0	1	10	0	N	0	0	10	E	5	0	0	10	0	0
82	B-2	N	6.5	0	A	0	0	M	O N			0	0	1	10	0	N	0	0	10	E	10	0	0	10	0	0
83	VCA	N	6.5	0	A	0	0	M				0	0	1	10	0	N	0	0	10	E	10	0	0	0	0	0
84	VCF	N	6.5	0	A	0	0	M				0	0	1	3	10	N	0	0	0	E	10	0	0	10	0	0
85	PWM	N	2	0	A	0	10	M	O N			0	0	1	10	0	N	0	0	10	E	10	0	0	10	0	0
86	LF01	N	6.5	0	M	10	0	M	O N			0	0	1	10	0	N	0	0	10	G	10	0	0	10	0	0
87	LF02	N	6.5	0	M	0	0	M				0	0	1	3.5	10	N	0	10	0	E	10	0	0	10	0	0
88	ENV	N	6.5	0	A	0	0	M	O N			0	0	1	10	0	N	0	0	10	E	10	10	0	0	0	0
91	VCFH	D	6.5	0	A	0	0	M				0	0	1	10	10	N	0	0	10	E	10	0	0	10	0	0
92	VCFL	N	6.5	0	A	0	0	M				0	0	1	0	10	N	0	0	10	E	10	0	0	10	0	0
93	VCFE	N	6.5	0	A	0	0	M				0	0	1	0	10	N	10	0	0	E	10	0	0	10	0	0
94	VCFE	N	6.5	0	A	0	0	M				0	0	1	10	10	R	10	0	0	E	10	0	0	10	0	0
95	DCO	N	2	0	A	10	0	M	O N			0	0	1	10	0	N	0	0	10	E	10	0	0	10	0	0
96	D-A	N			A			M	O N					1			N				E						0
97	OOH	-	0	10	A	0	0	L				0	0	1	0	0	N	0	0	0	G	0	0	0	0	0	0
98	OFFH	D	10	0	M	10	10	-	O N	O N	O N	10	10	3	10	10	R	10	10	10	E	10	10	10	10	10	3

Table 6 Panel Control Settings by Test Program

ADJUSTMENT PROCEDURES

1. POWER SUPPLY VOLTAGE (POWER SUPPLY BOARD)

Use a digital voltmeter with a resolution of millivolt.

- Adjust VR1 for $+15V \pm 10mV$ at "a".
- Check the voltage at "b". It should be $-14.5V$ to $-15.5V$.
- Check the voltage at "c". It should be $+4.5V$ to $+5.5V$. Refer to Fig. 24.

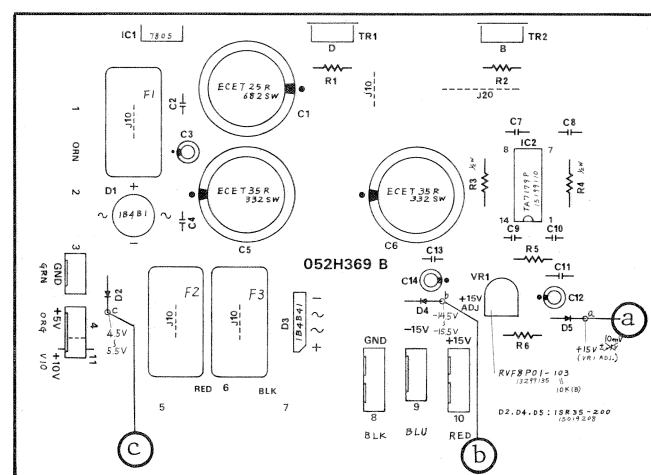


Fig. 24

2. MASTER OSCILLATOR (CPU BOARD)

2-1. BIAS

Test Point: TP2

- Connect digital voltmeter to TP2.
- Adjust VR39 for $+7.70V$.

2-2. TUNE

Test Point: OUTPUT
Patch Number: 82
Test Mode: UP
Control: TUNE (REAR PANEL) = center

- Connect Tuner, strobe, or other suitable equipment to OUTPUT jack.
- Hold down A4 key and adjust L1 for 442Hz using a nonferrous tool.

3. BENDER (BENDER BOARD)

Test Point: OUTPUT
Patch Number: 82

Note: Check to see if Edit Mark is ON. If so, select another Patch Number and again select "82" (see "Patch Number" section).

Test Mode: UP
Control: DCO (BENDER PANEL) = 10
(1) Connect proper tuning system to OUTPUT.
(2) Press HOLD.
(3) Press E5 key. Hold BENDER lever in leftmost position and adjust -ADJ VR1 for 442Hz. Press HOLD to release.
(4) Press HOLD again. Press D4 key.
(5) With BENDER lever in rightmost position, adjust +ADJ VR2 for 442Hz.

4. SAWTOOTH (CPU BOARD)

Test Point: CH1 TP3 (Rightmost TP3 on CPU BOARD)
Patch Number: 82
Test Mode: UP
Controls: HOLD = ON
OCTAVE TRANSPOSE = DOWN

Note: If OCTAVE TRANSPOSE is already in DOWN, reset it to NORMAL or UP, then to DOWN. This is for editing (see "Edit Mode" section).

- Press C2 key and adjust VR38 for 12Vp-p.
- Press C7 key and adjust VR37 for 12Vp-p.
- Press other key(s), and confirm $12V \pm 1Vp-p$.

Note: Reset OCTAVE TRANSPOSE to NORMAL for the remaining adjustments.

Caution: This adjustment will affect item 9, the PWM ADJUSTMENTS.

5. VCA (CPU BOARD)

5-1. GAIN

Test Point: TP4 pins 1-6 (CH1-CH6)
Patch Number: 82
Test Mode: UP
Control: HOLD = ON

- Connect oscilloscope to TP4 pin 1 (CH1).
- Press C4 key and adjust VCA GAIN VR4 of CH1 for 4Vp-p.
- Repeat steps (1) and (2) for TP4 pins 2-6 (CH2-CH6).

5-2. OFFSET

Test Point: TP4 pins 1-6 (CH1-CH6)
Patch Number: 83
Test Mode: UP

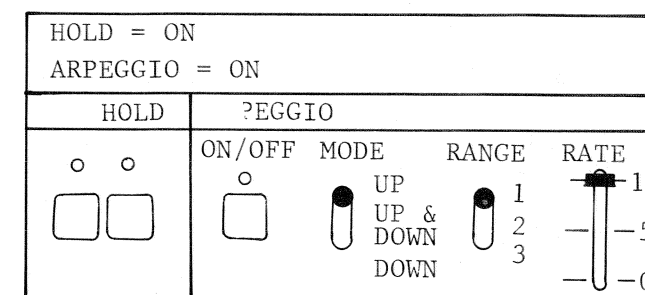


Fig. 25

- Connect oscilloscope (with V gain at maximum) to TP4 pin 1 (CH1).
- While pressing any two keys, adjust OFFSET VR5 of CH1 so that the pulses are minimized. (Fig. 26)
- Repeat steps (1) and (2) for TP4 pins 2-6 (CH2-CH6).

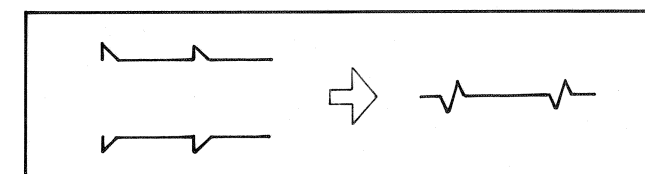


Fig. 26

- Press HOLD and ARPEGGIO OFF.

6. NOISE (CPU BOARD/PANEL BOARD A)

Caution: While adjusting PANEL BOARD A, use a screwdriver with a short shank to avoid short-circuiting to the heat sink of the POWER SUPPLY BOARD.

Test Point: TP4 (CPU BOARD)
Patch Number: 82
Controls: NOISE = 10
[] (PWM) = OFF

While pressing any key, adjust NOISE LEVEL VR14 (PANEL BOARD A) for 4Vp-p. (Fig. 27)

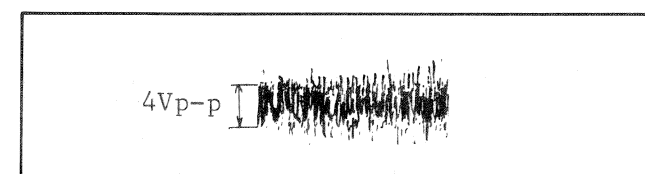


Fig. 27

7. LFO (PANEL BOARD A)

Preset the following controls for LFO adjustments unless otherwise specified.

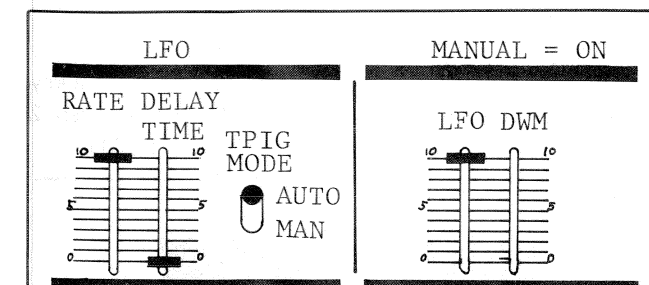


Fig. 28

Test Point: TP19 (PANEL BOARD A), Terminal 36 (PANEL BOARD A) or Terminal 20 (BENDER BOARD)

7-1. RATE

- Set oscilloscope to 10ms/cm, 2V/cm.
- Adjust LFO RATE VR1 for 45ms. (Fig. 29)

7-2. GAIN

- Set oscilloscope to 10ms/cm, 2V/cm.
- Adjust DCO LFO GAIN VR2 for 14Vp-p. (Fig. 29)

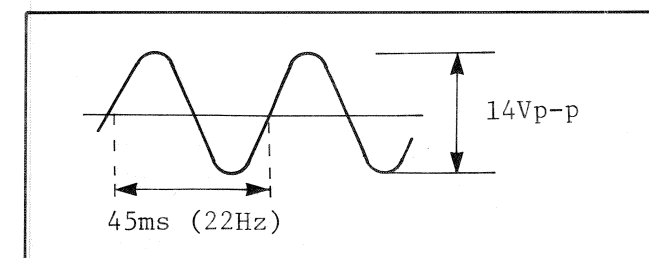


Fig. 29

7-3. OFFSET

- Set oscilloscope V gain at maximum.
- Set TRIG MODE to MAN (Manual).
- Adjust DCO LFO OFFSET VR3 so that the horizontal line rests on the GND potential. (Fig. 30)

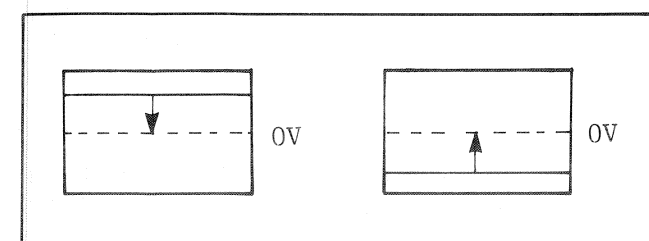
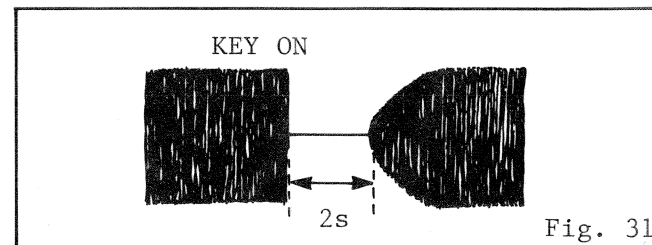


Fig. 30

7-4. DELAY

Note: HOLD must be OFF.

- (1) Reset TRIG MODE to AUTO. Set DELAY TIME to "10".
- (2) Set oscilloscope to 2V/cm, 0.5s/cm.
- (3) Adjust DELAY TIME VR4 so that when a key is pressed, the waveform disappears, then 2 seconds later, begins to reappear. (Fig. 31)



8. VCF (CPU BOARD/PANEL BOARD A)

Note: VCA adjustments must have been completed.

Caution: Items 8-1 through 8-5 must be adjusted in sequence.

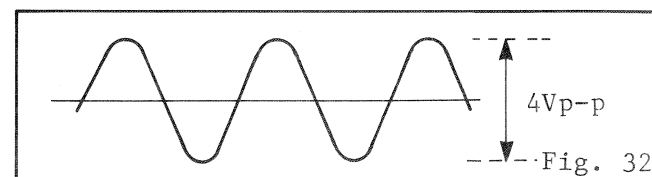
8-1. RESONANCE

Test Point: TP4 pins 1-6 (CH1-CH6) (CPU BOARD)

Patch Number: 84

Test Mode: UP

- (1) Connect oscilloscope to TP4 pin 1 (CH1).
- (2) Press any key and adjust RES VR1 (CPU BOARD) for 4Vp-p. (Fig. 32)
- (3) Repeat steps (1) and (2) for TP4 pins 2-6 (CH2-CH6).



8-2. FREQUENCY

Test Point: TP4 pins 1-6 (CH1-CH6) (CPU BOARD)

Patch Number: 84

Test Mode: UP

Note: FREQ VR2 of CH1 (CPU BOARD) should not be set too close to FCW or FCCW position.

- (1) Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
- (2) Press any key and adjust 248Hz ADJ VR5 (PANEL BOARD A) for 248Hz (=B3 note).
- (3) Repeat steps (1) and (2) for TP4 pins 2-6 (CH2-CH6) reading 248Hz ADJ VR5 as FREQ VR2 of CH2-CH6 (CPU BOARD).

8-3. KYBD OFFSET

Patch Number: 84

Test Mode: UP

Note: Either method (I) or (II) can be used as desired.

(I) Test Point: TP4

- (1) Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
- (2) Press C4 key.
- (3) Set KYBD to "10" and adjust KYBD OFFSET VR11 (PANEL BOARD A) for 248Hz.

(II) Test Point: VR3 HOT (TP-VCF CV IN) (CPU BOARD)

Control: HOLD = ON

- (1) Press C4 key.
- (2) While repeatedly moving KYBD to "10" and "0", adjust VR11 (PANEL BOARD A) so that the voltage variation is minimized.

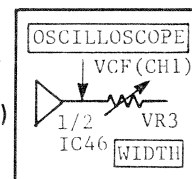


Fig. 33

Note: This adjustment can be made by listening to the sound from the Amp through the OUTPUT jack. Set ARPEGGIO to UP & DOWN or to DOWN. If necessary, HOLD should be turned OFF to silence the unneeded channel.

8-4. KYBD GAIN

Test Point: TP4 pin 1 (CH1) (CPU BOARD)

Patch Number: 84

Test Mode: UP

Control: KYBD = 10

Note: WIDTH VR3 of CH1 (CPU BOARD) should not be set too close to FCW or FCCW position.

- (1) Connect either Tuner or frequency counter to TP4 pin 1 (CH1).
- (2) Press C6 key and adjust KYBD GAIN VR10 (PANEL BOARD A) for 992Hz (B5 note).

8-5. WIDTH

Caution: Items 8-1 through 8-5 must be adjusted in sequence.

Test Point: TP4 pins 2-6 (CH2-CH6) (CPU BOARD)

Patch Number: 84

Test Mode: UP

Control: KYBD = 10

- (1) Connect either Tuner or frequency counter to TP4 pin 2 (CH2).
- (2) Press C6 key and adjust WIDTH VR3 of CH2 (CPU BOARD) for 992Hz.
- (3) Repeat steps (1) and (2) for TP4 pins 3-6 (CH3-CH6).

8-6. VCF LFO OFFSET

Test Point: OUTPUT

Patch Number: 87

- (1) Hold any key down.
- (2) Quickly slide LFO up and down and adjust VCF LFO OFFSET VR9 (PANEL BOARD A) so that the pitch does not vary.

8-7. VCF LFO GAIN

Test Point: VR3 HOT (TP-VCF CV IN) (CPU BOARD)

Patch Number: 87

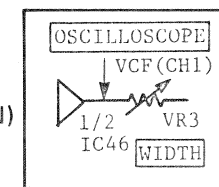


Fig. 34

With LFO TRIG pressed, adjust VCF LFO GAIN VR8 (PANEL BOARD A) for 6Vp-p.

Note: When observed at the OUTPUT jack, the frequency should vary between 40-50Hz and 4-5kHz.

8-8. VCF ENV OFFSET

Test Point: OUTPUT or TP4 (CPU BOARD)

Patch Number: 84

Controls: VCA ENV/GATE = GATE
ENVS = 0
(Refer to "Edit Mode" section.)

- (1) Press any key.
- (2) Quickly slide ENV (VCF) up and down and adjust VCF ENV OFFSET VR13 (PANEL BOARD A) so that the frequency does not vary.

Note: When TP4 is used as the test point, adjust VR13 so that the waveform is stable, or without jitter.

8-9. VCF ENV GAIN

Test Point: TP4 pin 1 (CH1) (CPU BOARD)
Patch Number: 93

Press any key and adjust VCF ENV GAIN VR12 (PANEL BOARD A) for approx. 30kHz. (T = approx. 34μs). (Fig. 35)

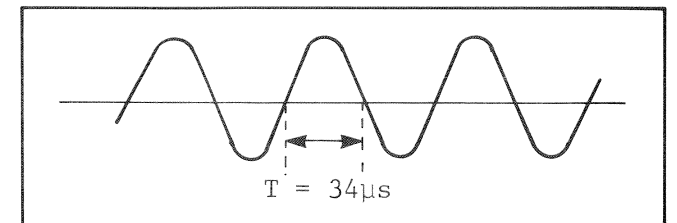


Fig. 35

9. PWM (CPU BOARD/PANEL BOARD A)

Note: Before this adjustment, the Sawtooth Adjustment must have been completed.

9-1. PWM 50%

Test Point: TP4 pins 1-6 (CH1-CH6) (CPU BOARD)

Patch Number: 82

Test Mode: UP

- (1) Connect oscilloscope to TP4 pin 1 (CH1).
- (2) Press C4 key and adjust PWM 50% VR6 (PANEL BOARD A) so that duty ratio of pulse is 50%. (Fig. 36)

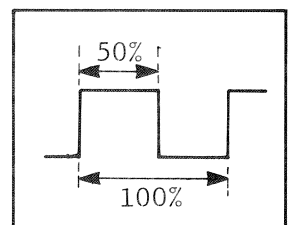


Fig. 36

- (3) Connect oscilloscope to TP4 pins 2-6 (CH2-CH6), and confirm that duty ratios are 47-50%.

9-2. PWM 95%

Test Point: TP4 CH1 (CPU BOARD)
Patch Number: 85

- (1) Connect oscilloscope to TP4 pin 1 (CH1).
- (2) Press C4 key and adjust PWM 95% VR7 (PANEL BOARD A) so that duty ratio is 95%. (Fig. 37)

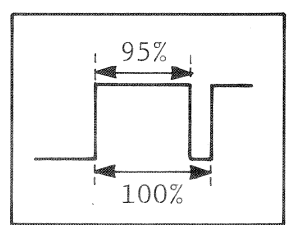


Fig. 37

10. ENVELOPE (CPU BOARD)

Test Points: TP6 pin 1 and TP7
Patch Number: 88
Test Mode: UP

- (1) Disconnect 10P- and 5P-connectors (connected to ports WR through RESET) on rightmost side of CPU BOARD.
- (2) Connect oscilloscope (2V/cm, 0.5s/cm) to TP6 pin 1.
- (3) Adjust ENV TIME VR6 of CH1 for 3-second attack time from pressing of key. (Fig. 38)

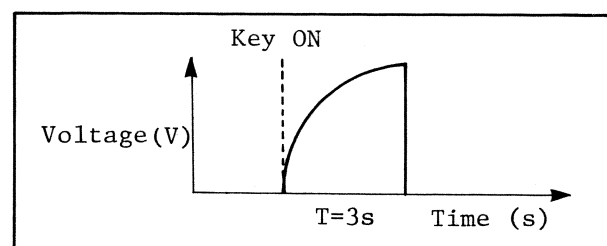


Fig. 38

- (4) Reconnect oscilloscope to TP7. Reset oscilloscope time base to 50μs/cm.
- (5) Holding down any key will display six growing waves on oscilloscope; CH1 being at leftmost position. Align rise time of remaining waves to CH1 rise time (coincidental max. to 0 transitions is desired.) (Fig. 39)

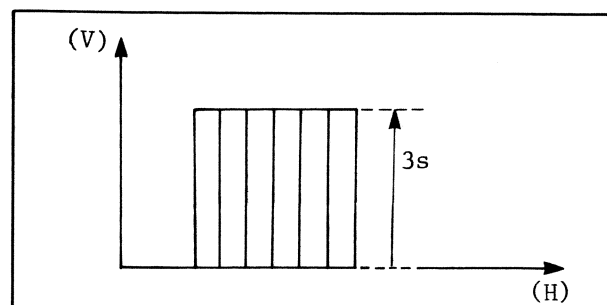


Fig. 39

- (6) Check 6 sounds for synchronization in A, D, S and R phases by sweeping respective sliders.

Note: After adjustment, reconnect the connectors.

Note: CHORUS BOARD is located under BENDER BOARD.

Test Points: TP1
TP2

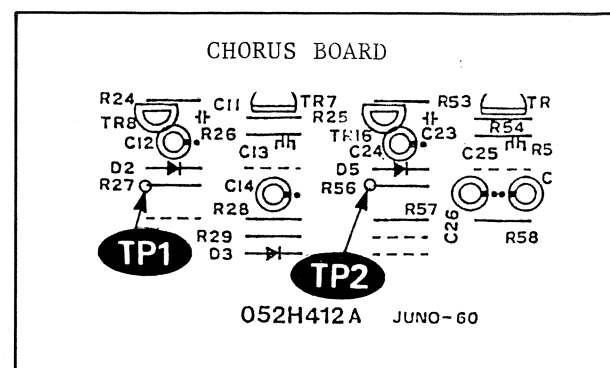


Fig. 40

Controls: MANUAL = ON
VCA LEVEL = Approx. 0
CHORUS = I

- (1) Feed test signal (6Vp-p, 1kHz, SINE) to TP8 (CPU BOARD).
- (2) Connect oscilloscope to TP1.
- (3) Adjust BIAS VR1 (CHORUS BOARD) so that top and bottom portions of waveform are not clipped. (Fig. 41)

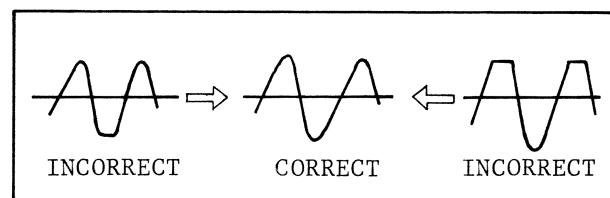


Fig. 41

- (4) Reconnect oscilloscope to TP2.
- (5) Adjust BIAS VR2 (CHORUS BOARD) so that top and bottom portions of waveform are not clipped. (Fig. 41)

PARTS LIST

CASES

081H261A	Cabinet	
083H052	Side panel	(right)
083H053	Side panel	(left)
072H132C	Top panel	
072H111A	Bender panel	
064H184	Holder Black	
or	(DCB connector)	
064H164	Nickel	
065H121A	LED Display window	
	Rubber foot G-5	

KNOBS, BUTTONS

22470128	Knob	(VOLUME)
016H004	Knob	(slide Pot, SW)
016H029	Button(orange)	SUT11A-1/2
016H030	Button(yellow)	SUT11A-1/2
016H036	Button(white)	SUT11A-1/2
016H037	Button(orange)	KEJ10901
016H038	Button(yellow)	KEJ10901
016H043	Button(gray)	KEJ10901
016H044	Button(white)	KEJ10901
	Key top (ivory)	KT3-2
	(See KEY SWITCH UNITS.)	

POWER SWITCH

13149108	WK2A44
or	
14149102	1801-0121

PUSH SWITCHES

(without button)		
13129321	SUT11A-1	momentary
13129322	SUT11A-2	maintained
13169605	KEJ10901	DCO, MEMO, TAPE, CHORUS

LEVER SWITCHES

13139136	SLE-622-18P	DPDT
13139135	SLE-623-18P	DP3T

SLIDE SWITCHES

13159332	HSW0372-01-520	
		MEMORY PROTECT
13159505	EVA-A03C14AGA	HPF FREQ

KEY SWITCH UNITS (LFO, TRIG)

(See p. 13 for detail.)

13129717	KEH10003	ass'y
13129714	KEH10903	switch proper
13129719	CHC32801A	guide pin
22269208	CK42602A	rubber cushion
12479703	KT3-2	key top

PCBs

149H161C	CPU BOARD	OPH161C
	(pcb 052H370C)	
149H187C	PANEL BOARD A	OPH187C
	(pcb 052H410C)	
149H188C	PANEL BOARD B	OPH188C
	(pcb 052H411C)	
149H194A	LED BOARD A	OPH194A
	(pcb 052H415A)	
149H162A	BENDER BOARD	OPH162A
	(pcb 052H371A)	
149H189A	CHORUS BOARD	OPH189A
	(pcb 052H412A)	
149H190A	JACK BOARD	OPH190A
	(pcb 052H413A)	
146H094B	POWER SUPPLY BOARD	
		PSH094B
	(pcb 052H369B)	100/117V
146H095B	POWER SUPPLY BOARD	
		PSH095B
	(pcb 052H369B)	220/240V
146H092A	FUSE BOARD	PSH092A
	(pcb 052H414A)	100/117V
146H093A	FUSE BOARD	PSH093A
	(pcb 052H414A)	220/240V

JACKS

13449708	ELJ0522-01-10(twin, mono)
13449224	HLJ2315-01-20 (stereo)

CONNECTORS

13429611	57-4014-R
	DCB (connector) socket
012H026	5714S DCB connector cap

FUSES

12559331	GG5-0.8A	pri.(100/117V)
12559511	CEE T500mA	pri.(220/240V)
12559513	CEE T1.0A	sec.(220/240V)

BENDER UNIT

029-022	PB-4 or PB-8
	(compatible)

POSISTORS

15229909	ERS-B33G561	560
15229910	ERS-B33G122	1.2k

RESISTOR ARRAYS

13829821	RGSD 8 x 103k	10k x 8
13910113	RGSD 4 x 103k	10k x 4
13910114	RGSD 4 x 223k	22k x 4
13919117	RGSD 8 x 333k	33k x 8
13919118	RK600601611	
	or RGSD16L104G	
	Ladder Network	

PARTS LIST

POTENTIOMETERS

Slider

13339410	EVA-TOHC14A54	50kA
13339419	EVA-TOHC14B54	50kB
13339418	EVA-TOHC14A16	1MA
13339416	EVA-TOHC14A14	10kA

Rotary

13219759	EWJ-EJAP20B14	10kB x 2
13219401	EVH-OTAS15B14	10kB (TUNE)

Trimmer

13299134	RVF8P01-502	5kB
13299135	RVF8P01-103	10kB
13299169	RVF8P01-203	20kB
13299136	RVF8P01-503	50kB
13299137	RVF8P01-104	100kB
13299553	RVS0707V101-102M (BUL)	1kB
13299554	RVS0707V101-502M (BUL)	5kB

COIL

022A018	S167999	37μH
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POWER TRANSFORMER

022H057	(100/117/220/240V)
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DIODES

15019103	1S2473 or 1S1555
15019243	1B4B1 (rectifier bridge)
15019245	1B4B41 (rectifier bridge)
15019249	KV1226-X or Y (varicap)
15029103	TLR-124 (LED) red
15029141	LT-8001P (LED) used as a zener
15029404	LN526RA (LED) display
or	
15029410	LB602VA2

ICs

IMPORTANT:
REPLACEMENTS FOR SELECTIVELY USED
SEMICONDUCTORS

Some semiconductors exclusive to the JUNO-60 are selected among various equivalents, even from the same brand to meet design requirements. Correct replacement can be obtained only when these specialities are distinguished in the order sheet.

Expls:

151793050A	μPD444C-1 only (JUNO-60)
15179147	μPD8049C-380 replacement for -238 version(JUNO-60)

Also identify the model "JUNO-60" to imply the reason for ordering special semiconductors.

15179135	μPD8049C-238 CPU
or	(CPU BOARD)

15179147	μPD8049C-380
	For replacement, use 380 version.
	See p. 9 for necessary modification.

15179137	μPD8049C-028 CPU
	(PANEL BOARD B)

15179311	TC5514AP-3
	1024 x 4 bit or CMOS

or	Static RAM
151793050A	μPD444C-1 (selected)
	For replacement, use μPD444C-1
15179327	or TC5513AP-20.

15179110	μPD8253C-5 or MSL8253P-5
	Triple Programmable

15179138	μPD8251AC or MSL8251AP
	Programmable Communica-
	tions Interface

15159503	TC40H000P
	Quad 2-Input NAND Gate

15159504	TC40H002P
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	Quad 2-Input NOR Gate
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15159505	TC40H004P
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	Hex Inverter
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15159506	TC40H138P
----------	-----------

	3-to-8 Line Decoder/ Demultiplexer
--	---------------------------------------

15159507	TC40H273P
----------	-----------

	Octal D-type Flip-Flop
--	------------------------

15159508	TC40H373P
----------	-----------

	Octal D-type Latch
--	--------------------

15159509	TC40H393P
----------	-----------

	Dual 4-bit Binary Counter
--	---------------------------

15159104H0	HD4011B
------------	---------

	Quad 2-Input NAND Gate
--	------------------------

15159105H0	HD14013B
------------	----------

	Dual D-type Flip-Flop
--	-----------------------

15159112H0	HD14049B
------------	----------

	Hex Inverter/Buffer
--	---------------------

15159128H0	HD14050B
------------	----------

	Hex Buffers
--	-------------

15159113H0	HD14051B
------------	----------

	Single 8ch Multiplexer
--	------------------------

15159115T0	TC4066B
	Quad Analog Switch
15159116T0	TC4069UB
	Hex Inverter
15159120T0	TC4099B
	Quad Analog Switch
15159133T0	TC40174B
	Hex D-type Flip-Flop
15169117	7407 or MS307P
	Hex Buffers/Drivers
15169341	74LS14
	Hex Schmitt Trigger
	Inverters
15169310	74LS42
	BCD-to-Decimal Decoder
15219125	M54528P
	7-Segment Driver
15189119	TL062CP
	OP Amp
15189118	HA17082PS/NJM082D,
	μPC4082C or TL082CP
	OP Amp
15189148	NJM072S
	J FET Input Dual OP Amp
15189111	NJM311D or μPC311C
	Voltage Comparators
15189136B0	M5218L
	OP Amp
15189142	TA75558S
	OP Amp
15189105N0	μPC4558C
	OP Amp
15229801	IR3109
	VCF
15229807	IR3R01
	ADSR
15229802	BA662A
	VCA
15189143	TA75559S
	Dual OP Amp
15219213	MN3009
	BBD
020-224	MN3101
	BBD Driver
15219124	μPC1252H2 (VCA)
15199106	AN7805
	+5V Voltage Regulator
15199110T0	TA7179P
	15V Voltage Regulator

CAPACITORS

13659223M0	ECET35R332SW	3300μF/35V
13659224M0	ECET25R682SW	6800μF/25V
13589461	ECQ-U1A473MH	0.047μF
	polypropylene	

TRANSISTORS

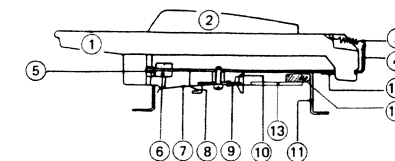
15119805	2SB834-0 or Y
15129816	2SD880-0 or Y
15119113	2SA1015-GR or Y or
	15119124, 2SA115-GR or Y
15129117	2SC1923-0 or Y
	or 2SC381-R
15129128	2SC752-G or O
15129114	2SC1815-GR or Y or
	15129135, 2SC2603-GR or Y
15129130	2SC1583-F or G
151291080A	2SC945 SELECTED FOR NOISE
15119601	2SB605-K or L
	or 2SB926-S or T
15129600	2SD571-L2A
15139103	2SK30A-GR or Y (FET)
15129136	2SC2878-A or B

OTHERS

12389801	KMFC1002T	4MHz
	(Ceramic resonator CSA	
	4MHz and paired CSC300)	
12389800	KMFC1005T1	6MHz
	(Ceramic resonator CSA	
	6MHz and paired CSC300)	
12389807	KMFC1037T	11MHz
	(Ceramic resonator CSA	
	11MHz and paired CSC300)	
12569111	CR-1/3N	3V Litium battery

KEYBOARD

004H008	SK-361C	(61 keys)
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KEYBOARD PARTS
SK-361C (004H008)

NO	PART NO	DESCRIPTION
1	106H026	Natural key C F
1	106H027	Natural key D
1	106H028	Natural key E B
1	106H029	Natural key G
1	106H030	Natural key A
1	106H031	Natural key C' F'
2	106H032	Sharp key black
3	070H029	Key spring H29
4	061H086A	Chassis H86A
5	068H004	Guide bushing H4
6	101H141	Level felt H141
7	071H044	Contact leaf H44
8	071H051	Busbar 8P H51
8	071H054	Busbar 5P H54
9	043H007	Switch unit 12P H7
9	043H008	Switch unit 13P H8
10	104H029	Busbar holder H29
11	062H024	Chassis bracket H24
12	098H006	Key stopper H6
13	052H283-5	Matrix board H283-5
14	107H059	Cushion H59